|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **EE222 Winter 2017 Quarter** | Topic | Textbook\*Read | HW | Reference# |
| 1. Jan. 9 T
 | Introduction | Ch1 (pp.1-48) | HW1:Prob.1.1(for part b, use the Fig. on p.48), 1.3  | R1(pp.1-23), R2(pp.1-27) |
| 1. Jan. 11 Th
 | MOS Transistors (MOSTs) | Ch3 (pp.51-78) | HW2:Prob.3.1, 3.6, 3.14 |  |
| 1. Jan. 16 T
 | Short channel MOSTs | Ch3 (pp.83-120) |  | R1(pp.25-52)R2(pp.129-154) |
| 1. Jan. 18 Th
 | Modeling of MOSTs (SPICE), EKV model | Ch4 (pp.125-150) | HW3:Prob.4.1, 4.3 | R2(pp.130-133) |
| 1. Jan. 23 T
 | CMOS Inverters | Ch6 (pp.153-175) | HW4:Prob.6.2, 6.3 |  |
| 1. Jan. 25 F
 | Interconnects | Ch6 (pp.176-196) | HW5:Prob.6.8 | R1(pp.151-161) |
| 1. Jan. 30 T
 | Power, EnergySuper buffer Design | Ch6 (pp.196-208) |  | R1(pp.53-75) |
| 1. Feb. 1 Th
 | Memories-DRAM | Ch10(pp.213-247) | HW6:Prob.10.1, 10.2 |  |
| 1. Feb. 6 T
 | Midterm Exam 1 |  | Project Proposal |  |
| 1. Feb. 8 Th
 | Memories-SRAM | Ch10(pp.247-263) |  | R1(pp.183-205, 233-247)) |
| 1. Feb.13 T
 | NVMs (ROM, FLASH, FRAM, STT-RAM, PCRAM. RRAM | Ch10(pp.263-287) | HW6:Prob.10.3, 10.4, 10.6 |  |
| 1. Feb.15 Th
 | (continued) |  |  |  |
| 1. Feb.20 T
 | LP CMOS Logic Circuits | Ch11(pp.293-313) | HW7:Prob.11.2, 11.4 |  |
| 1. Feb.22 Th
 | Pipelining, Parallel Processing, Adiabatic Circuits | Ch11(pp.313-333) |  | R2(pp.642-647) |
| 1. Feb.27 T
 | I/O Circuits, Clocking, Multiple Vdd and Level Shifting | Ch13(pp.336-371) | Prob.13.1, 13.3, 13.9 | R1(pp.92-97) |
| 1. Mar.1 Th
 | Ultra Low Power (ULP) Design and Subthreshold Circuits |  |  | R1(289-315)R2(pp.618-630) |
| 1. Mar.6 T
 | 2nd Half Midterm |  |  | R2(697-705, 739-749 |
| 1. Mar. 8 Th
 | More on advanced topics in LP |  |  | R2(697-705, 739-749), etc. |
| 1. Mar.13 T
 | Project Presentations |  | Submit written reports |  |
| 1. Mar.15 Th
 | Project Presentations |  | Submit Written Reports |  |
|  |  |  |  |  |
|  |  |  |  |  |
| FINAL scheduled on Mar. 22 (4-7 p.m.) | Replaced by Project Presentations |  |  |  |
|  |  |  |  |  |

\*Textbook S. M. Kang, et al. CMOS Digital Integrated Circuits Analysis and Design,

UCSC version- UCSC version (2017)

#Ref.1 (R1) J. Rabaey, Low Power Design Essentials, Springer (2009)

#Ref.2 (R2) R. Sarpeshkar, Ultra Low Power Bioelectronics, Cambridge University Press (2013)

**EE222 Course Grading**

* HWs are assigned, but not collected for grading.
* Two midterms, 35% each toward final grade.
* Project evaluation counts 30%.

Course Project Guidelines

* Project can be a single-person project or a group project (each group up to three students).
* Project performance constitutes 30% of the overall evaluation.
* Evaluation is based on presentation (10%) and written report (20%).
* Possible Projects
	+ In-depth analysis and critique of recent low-power papers published in professional journals such as Journal of Solid-State Circuits (JSSC), IEEE Trans. On Circuits and Systems, IEEE Trans. On VLSI Systems, or conference papers in International Symp. on Physical Design (ISPD), International Solid-State Circuits Conference (ISSCC), Design Automation Conference (DAC), etc.
	+ For independent design of low power circuits; SPICE level simulation results would be sufficient.
	+ IoT, low-power neuromorphic circuits can be of special interest, also.